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A high voltage gain switched-capacitor DC-DC converter based on three parallel-connected Fibonacci converters

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Abstract

For use in energy harvesting systems with low voltages energy sources, this paper presents a high voltage gain converter using three parallel-connected Fibonacci converters. By using the parallel connected topology, the proposed converter can actualize a high voltage gain as the power of three. Moreover, owing to the parallel-connected structure, the total internal resistance is minimized. Therefore, the power efficiency of the proposed converter is better than that of traditional converters. Furthermore, unlike traditional converters, the step-up electric charge of the proposed converter is provided in all of the clock cycles. Hence, the proposed converter can connect with a small output capacitor, untroubled by ripple noise. For this reason, when the improved circuit is turned into a chip, the size of the proposed converter will be smaller than traditional converters.

Keywords: three parallel connected topologies; Fibonacci converters; switched-capacitor converters.

1. Introduction

There is a greater demand for energy due to growing populations worldwide. Failure to prepare for energy needs may cause future energy shortages. To prevent these problems, the research on clean energy harvesting [1-5] is essential. Along with the development of clean energy harvesting and energy conversion into electrical energy, another essential area of research will be creating high efficiency converters. A popular converter is the inductor converter, which has high power efficiency. However, the inductor converter has magnetic flux effect that makes it hard to reduce the circuit size. This paper proposes one of the forms of switched-capacitor (SC) dc-dc converters [6-8]. This can be improved to become a chip at the smallest possible size. The energy harvesting systems utilize small-scale energy sources, such as ambient vibrations, wind, heat, and light. Therefore, the converter should have a high voltage gain [9, 10]. In the past few decades, there have been a lot of researches about the SC converter. For example, Wang et al. researched the SC dc-dc converter for energy harvesting systems [11] as well as Yun et al. researched about a charge pump using a multivibrator for thermoelectric generators [12, 13]. However, the voltage gain of both converters is the stage times input voltage $N\times$ (N = 1, 2, 3 ...). As a result, the circuit size becomes large by connecting many stages to achieve a high voltage gain when used for energy harvesting systems from uncommon energy sources. Eguchi et al. developed about the Fibonacci SC dc-dc converter [14-17], even though the voltage gain of the Fibonacci converter can reach a very high level. However, a stepped-up electric charge of the output capacitor of the Fibonacci converter is evoked in a half clock cycle. As a result, a large output capacitor is required to reduce output ripple noise. This large output capacitor makes the size of the circuits large. Chang et al. suggested

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Variable-Conversion-Ratio Switched-Capacitor-Voltage-Multiplier/Divider (SCVM) [18-20] even though the structure of the SCVM converter can realize a high voltage gain easily with $N \times M$ (N, M = 1, 2, 3 ...). However, a stepped-up electric charge of the output capacitor of the SCVM converter is also evoked in an only half clock cycle. Therefore, a large output capacitor is necessary for the SCVM. Eguchi et al. suggested a design of a cross-connected charge pump for energy harvesting systems, where the voltage gain of the converter is $2NV_{in}$ (N = 1, 2, 3...) [21, 22]. The cross-connected charge pump can minimize the size of the output capacitor, because the stepped-up electric charge of the output capacitor is evoked in all of the clock cycles. However, the circuit size is able to become large by connecting many stages to make high voltages gain when harvesting energy from uncommon energy sources where voltages are normally small.

To overcome the above-mentioned problems, a three Fibonacci parallel connected SC dc-dc converter for energy harvesting system is proposed in this paper. The proposed converter can realize the high voltage gain, with $3N \times V_{in}$ (N= 1, 2, 3 ...), and minimize the circuit size by connecting with a small output capacitor. Furthermore, unlike conventional converters, the proposed converter can achieve small ripple noise. Therefore, the proposed converter is appropriate for energy harvesting systems. The assessment of the proposed converter is executed by theoretical analysis, simulation program with integrated circuit emphasis (SPICE) simulations, and experiments.

2. Circuit Configuration

2.1. Traditional fibonacci converter

Fig. 1 demonstrates the circuit configuration of the traditional Fibonacci converter with 4 stages. The transistor switch S1 and S2 are controlled by non-simultaneous two-phase clock pulses. The output voltage of the traditional Fibonacci converter is expressed as

$$V_{out} = V_n = V_{n-1} + V_{n-2}, \quad (N > 0). \tag{1}$$

The pattern of the output voltage of the traditional Fibonacci converter is a voltage of the last stage plus second to last stage. By the parameter N denotes an integer that shows the number of stages. When the parameter N is (N = 0, 1, 2, 3, 4), the output voltage of equation (1), becomes V_{in}, 2 V_{in}, 3 V_{in}, 5 V_{in}, and 8 V_{in}. A stepped-up electric charge of the output capacitor of the traditional Fibonacci converter is evoked in half clock cycles. Therefore, the traditional Fibonacci converter needs to connect with a large output capacitor C_{out} to minimize the ripple output. The traditional Fibonacci converter accomplishes high voltage gains easily, but at the cost of large circuit size and slow response speed. The traditional Fibonacci converter is inappropriate for energy harvesting systems from uncommon energy sources.

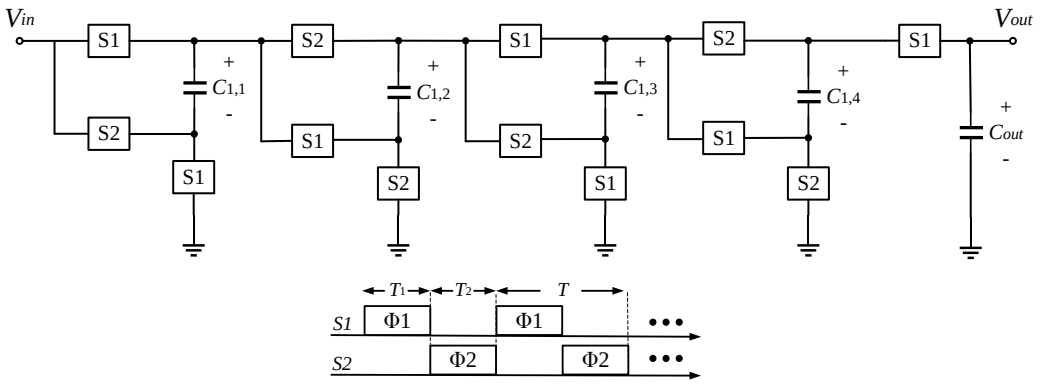


Fig. 1. Circuit configuration of the 4-stages traditional Fibonacci converter.

2.2. Proposed converter

Fig. 2 demonstrates the designed circuit of the proposed converter with 2 stages in the conversion ratio of 9. The transistor switch S1, S2, and S3 are controlled by non-simultaneous three-phase clock pulses (Φ1, Φ2, and Φ3). The output voltage of the proposed converter is demonstrated by

$$V_{out} = 3N \times V_{in}, \quad (\mathrm{N} > 0). \tag{2}$$

The pattern of the output voltage of the proposed converter is three with the exponent of the stage times the input voltage stage. By the parameter N denotes an integer that shows the number of stages. When the parameter N is (N = 1, 2, 3), the output voltage of "(2)," becomes 3 V_{in}, 9 V_{in}, and 27 V_{in}. "(1)," and "(2)," show the voltage gain of the Fibonacci traditional converter is much lower than the proposed converter when the number of stage N of both converters is identical. Although, the output capacitor of the proposed converter is not large, it is effective because the stepped-up electric charge of the output capacitor of the proposed converter is evoked in every clock cycle. Furthermore, by using a parallel-connected structure, the proposed converter can accomplish this with a small circuit size, high voltage gains, and fast response speed. The proposed converter is appropriate for energy harvesting systems.

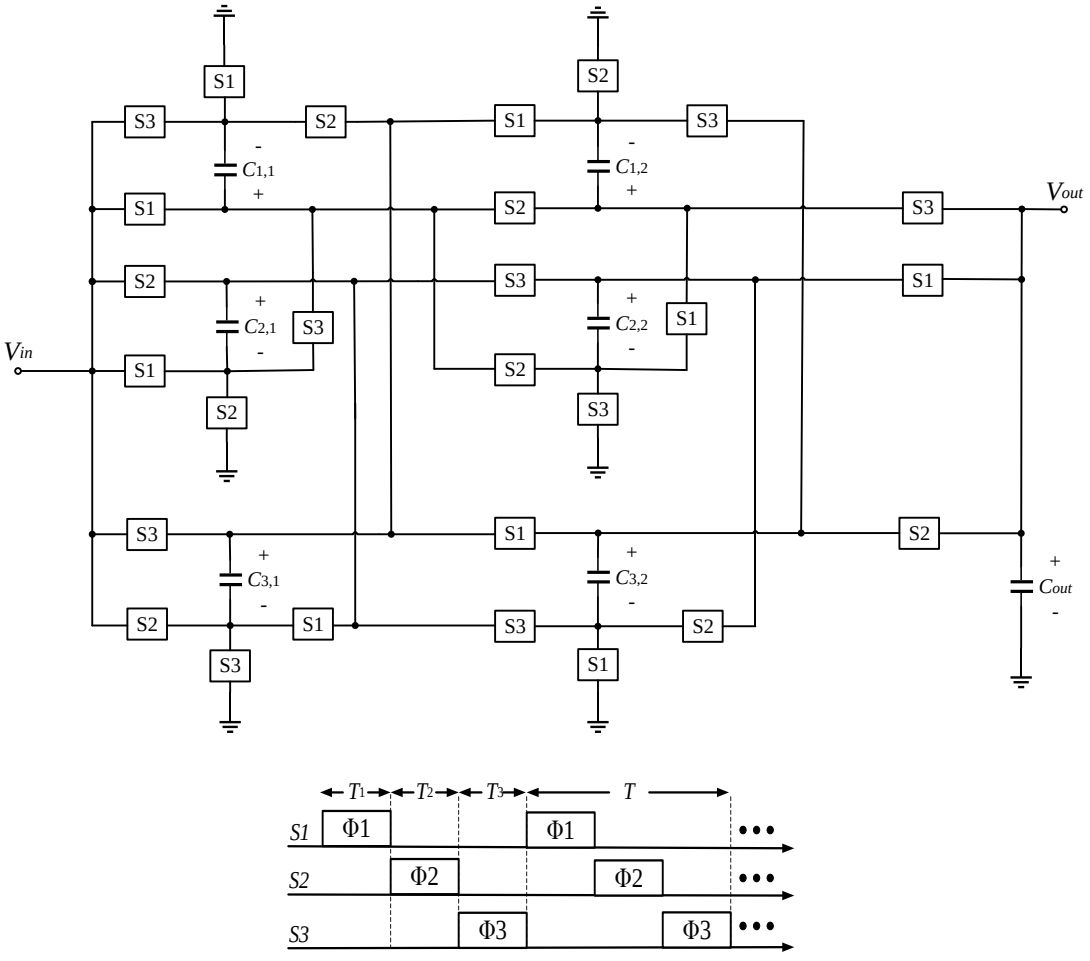


Fig. 2. Circuit configuration of the 2-stages proposed converter.

3. Theoretical Analysis

By designing a 2-stage structure to generated 9×step-up voltage gain, the proposed converter characteristic is analyzed theoretically to find the equation of the maximum power efficiency and internal total resistance by applying the four-terminal equivalent model [23, 24] as in Fig.4. In a steady state, the instantaneous equivalent circuits of the proposed converter are analyzed from Fig. 3, where Ron is a sign of an on-resistance of the transistor switch. In Fig 3, the aggregate of charged and discharged electricity of the capacitor is zero. The differential value of electric charges $\Delta q^{i,j}{}_{Ti}$ in $C_{i,j}$ (i = 1, 2, 3 and j = 1, 2) satisfies the following condition:

$$\Delta q^{i,j}{}_{T1} + \Delta q^{i,j}{}_{T2} + \Delta q^{i,j}{}_{T3} = 0, \tag{3}$$

In "(3)," the intervals T satisfy the following conditions:

$$T = T1 + T2 + T3 \quad \text{and} \quad T/3 = T1 = T2 = T3. \tag{4}$$

When switch S1 is on as in Fig. 3 (a), the differential value of electric charges in the input and the output, $\Delta q_{T1,Vin}$ and $\Delta q_{T1,Vout}$ are demonstrated as

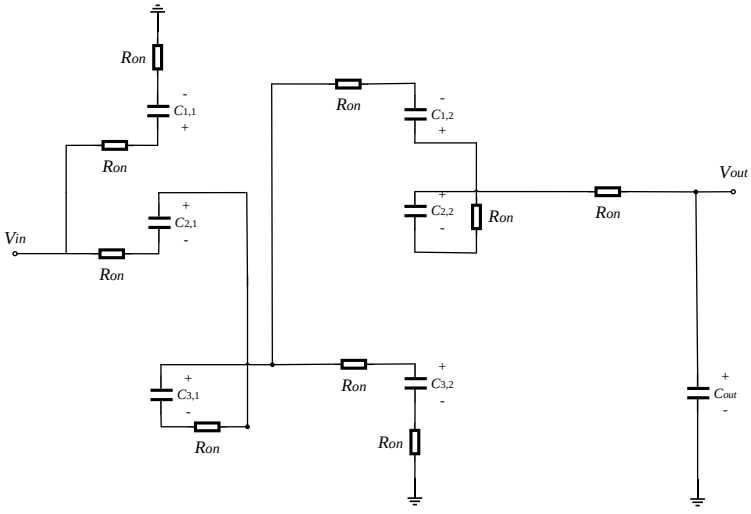
$$\begin{aligned}
\Delta q_{T1,Vout} &= \Delta q^{out}{}_{T1} + \Delta q^{2,2}{}_{T1},\\
\Delta q_{T1,Vin} &= \Delta q^{1,1}{}_{T1} - \Delta q^{2,1}{}_{T1},\\
\Delta q^{3,1}{}_{T1} &= \Delta q^{2,1}{}_{T1},\\
\Delta q^{1,2}{}_{T1} &= \Delta q^{3,2}{}_{T1} + \Delta q^{3,1}{}_{T1},\\
\Delta q^{2,2}{}_{T1} &= \Delta q^{1,2}{}_{T1},
\end{aligned} \tag{5}$$

When switch S2 is on as in Fig. 3 (b), the differential value of electric charges in the input and the output, $\Delta q_{T2,Vin}$ and $\Delta q_{T2,Vout}$ are demonstrated as

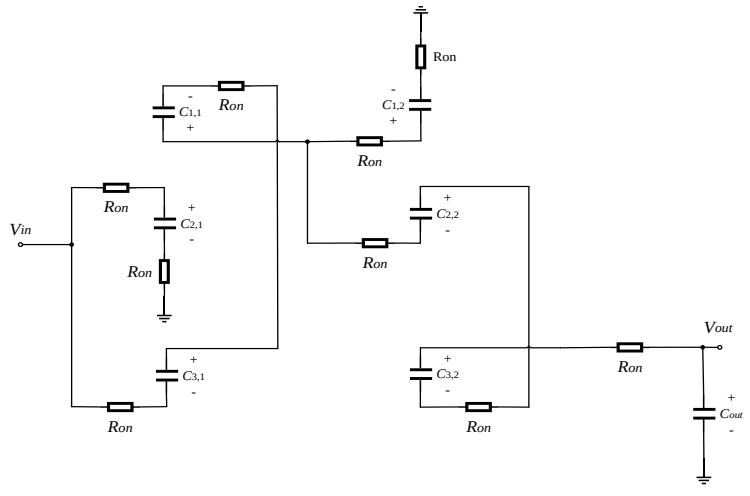
$$\begin{aligned}
\Delta q_{T2,Vout} &= \Delta q^{out}{}_{T2} + \Delta q^{3,2}{}_{T2},\\
\Delta q_{T2,Vin} &= \Delta q^{2,1}{}_{T2} - \Delta q^{3,1}{}_{T2},\\
\Delta q^{1,1}{}_{T2} &= \Delta q^{3,1}{}_{T2},\\
\Delta q^{2,2}{}_{T2} &= \Delta q^{1,1}{}_{T2} + \Delta q^{1,2}{}_{T2},\\
\Delta q^{3,2}{}_{T2} &= \Delta q^{2,2}{}_{T2},
\end{aligned} \tag{6}$$

When switch S3 is on as in Fig. 3 (c), the differential value of electric charges in the input and the output, $\Delta q_{T3,Vin}$ and $\Delta q_{T3,Vout}$ are demonstrated as

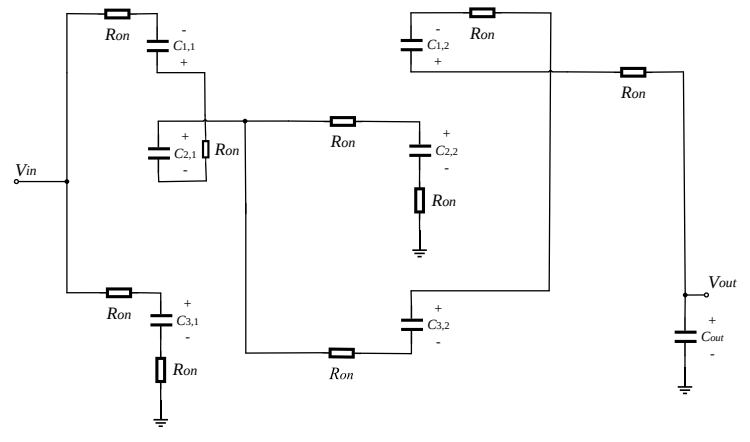
$$\begin{aligned}
\Delta q_{T3,Vout} &= \Delta q^{out}{}_{T3} + \Delta q^{1,2}{}_{T3},\\
\Delta q_{T3,Vin} &= \Delta q^{3,1}{}_{T3} - \Delta q^{1,1}{}_{T3},\\
\Delta q^{2,1}{}_{T3} &= \Delta q^{1,1}{}_{T3},\\
\Delta q^{3,2}{}_{T3} &= \Delta q^{2,1}{}_{T3} + \Delta q^{2,2}{}_{T3},\\
\Delta q^{1,2}{}_{T3} &= \Delta q^{3,2}{}_{T3},
\end{aligned} \tag{7}$$



(a)



(b)



(c)

Fig. 3. Instantaneous equivalent circuits: (a) state-T_1, (b) state-T_2, and (c) state-T_3.

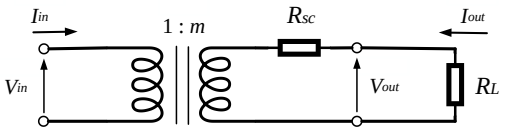


Fig. 4. Four-terminal equivalent model.

By using "(5)," - "(7)," the average input current I_{in} and the average output current I_{out} can be demonstrated as

$$I_{in} = \Delta q_{Vin} /T = (\Delta q_{T1,Vin} + \Delta q_{T2,Vin} + \Delta q_{T3,Vin})/T$$

$$\text{and} \quad I_{out} = \Delta q_{Vout} /T = (\Delta q_{T1,Vout} + \Delta q_{T2,Vout} + \Delta q_{T3,Vout})/T. \tag{8}$$

Δq_{Vin} and Δq_{Vout} are marks of electric charges in V_{in} and V_{out}, respectively. When substituting equations (3) - (7) into (8), the relationship between the average input current I_{in} and the average output current I_{out} can be demonstrated as

$$I_{in} = -9I_{out} \qquad \text{and} \qquad \Delta q_{Vin} = -9\Delta q_{Vout} \tag{9}$$

As a result of equation (9), the parameter m is equal to 9 in Fig.4, where $m = 9$.

Next, the used energy of the proposed converter is discussed for initial time period T_1 in order to achieve the value of parameter R_{SC} in Fig.4 by using Fig. 3 (a), the used energy when switch S1 is on is demonstrated as

$$W_{T1} = 2R_{on}(\Delta q^{1,1}{}_{T1})^2/ T_1 + R_{on} (\Delta q^{2,1}{}_{T1})^2/ T_1 + R_{on} (\Delta q^{3,1}{}_{T1})^2/ T_1 + 2R_{on} (\Delta q^{3,2}{}_{T1})^2/ T_1$$
$$+ R_{on} (\Delta q^{1,2}{}_{T1})^2/ T_1 + 2R_{on} (\Delta q^{2,2}{}_{T1})^2/ T_1 \tag{10}$$

By substituting "(3)," - "(7)," into "(10)," the total energy used can be described as

$$W_T = 101R_{on}(\Delta q_{Vout})^2/ T \tag{11}$$

On the other hand, the total energy used in Fig. 4 can be described as

$$W_T = R_{sc}(\Delta q_{Vout})^2/ T \tag{12}$$

From "(11)," and "(12)," the parameter R_{sc} in Fig. 4 is equal to 101/3 R_{on}. By combining the parameters R and R_{SC}, we have the equivalent circuit of the proposal converter by the K-matrix. Therefore, the maximum power efficiency η_{max} and the maximum output voltage V_{max} are described as follows:

$$\eta_{max} = R_L /(101R_{on} + R_L) \qquad \text{and} \qquad V_{max} = \{R_L /(101R_{on} + R_L)\} \times 9\ V_{in} \tag{13}$$

Equation (13) shows the equation of the key parameters η_{max} and V_{max}.

4. Comparison

Table (1) presents the comparison of the number of the circuit components of the proposed converter in the 9×step-up voltage gain with 2 stage structures and the traditional Fibonacci converter in 8×step-up voltage gain with 4 stage structures. Although the number of switches and capacitors of the proposed converter is more than the traditional Fibonacci converter, the stepped-up electric charge of the output capacitor of the traditional Fibonacci converter is evoked in only half clock cycles. Thus, the traditional Fibonacci converter needs to connect with a large output capacitor to minimize ripple noise. On the other hand, when improving circuits to be a chip, the area the capacitors occupy is bigger than the transistor switches. From the above-mentioned issue, the proposed converter circuit size is smaller. From Table (2), the power efficiency of the proposed converter is higher because the total internal resistance is less than

the traditional Fibonacci converter. Moreover, the voltage gain of the proposed converter is higher with 9. For this reason, the size, voltage gain and the efficiency of the proposed converter is better. Therefore, the proposed converter is appropriate for energy harvesting systems.

Table 1. Comparison of component counts

Converter topology	Number of switches	Number of capacitors
Fibonacci converter	13	5 + Big C_{out}
Proposed converter	27	7 + Small C_{out}

Table 2. Comparison of Characteristics

Converter topology	Voltage Gain	power efficiency η_{max}
Fibonacci converter	8	$\eta_{max} = R_L / (140R_{on} + R_L)$
Proposed converter	9	$\eta_{max} = R_L / (101R_{on} + R_L)$

5. Simulation

The simulations were set-up under the following conditions: the input voltage V_{in} = 400mV, the capacitance of both converters $C_{1,1} = \ldots = C_{3,2} =$ 500pF, the output capacitance of the proposed converter C_{out} = 500pF, the output capacitance of the traditional Fibonacci converter C_{out} = 10nF and 500pF, the value of frequency f = 20 MHz, Internal resistance R_{on} = 1. The first result is the simulated power efficiency as a function of the output power as Fig. 5. We found the power efficiency of both converters depended on the output power, lower output powers correlating with higher power efficiency. However, the power efficiency of the proposed converter always performed better than the traditional Fibonacci converters. The second result is the simulated output voltage as a function of the output power as Fig. 6. We found the output voltage of both converters resembled the results regarding power efficient in Fig. 5, but the output voltage of the proposed converter became much higher starting around 3.6 V, unlike the traditional Fibonacci converter, which started around 3.2 V. The third result is the simulated ripple voltage as a function of the output power as Fig. 7. We found the ripple voltage is depended on the output power. However, the ripple voltage of the Fibonacci converter which connecting with a small output capacitor is very high. The Fibonacci converter can solve the ripple noise problem by connecting with a large output capacitor. Unlike, the proposed converter which connecting with a small output capacitor though. Because of the stepped-up electric charge of the output capacitor is evoked in all of the clock cycles. The last result is the simulated output voltage as a function of time as in Fig. 8. Fig. 8 (a) is the result of the proposed converter and Fig. 8 (b) is the result of the traditional Fibonacci converter. The result shows the response speed of the proposed converter is very high when compared to the traditional Fibonacci converter.

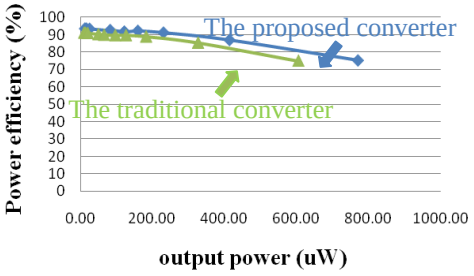


Fig. 5. Simulated power efficiency as a function of the output power.

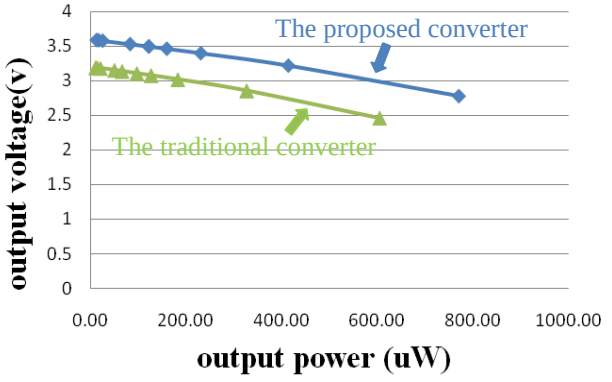


Fig. 6. Simulated output voltage as a function of the output power.

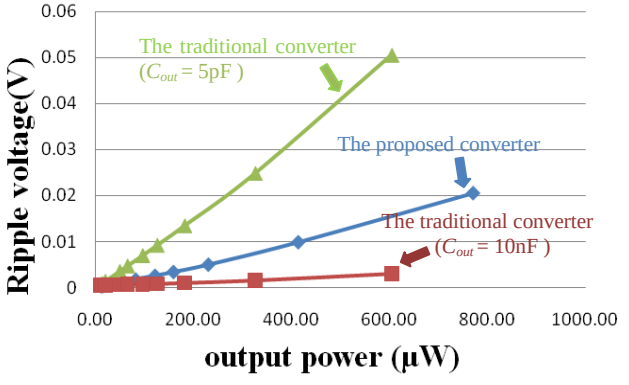
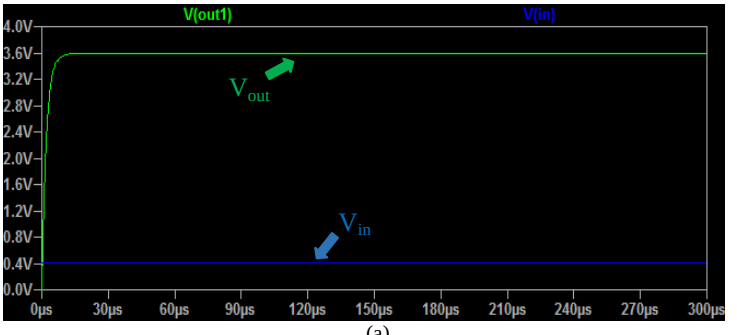
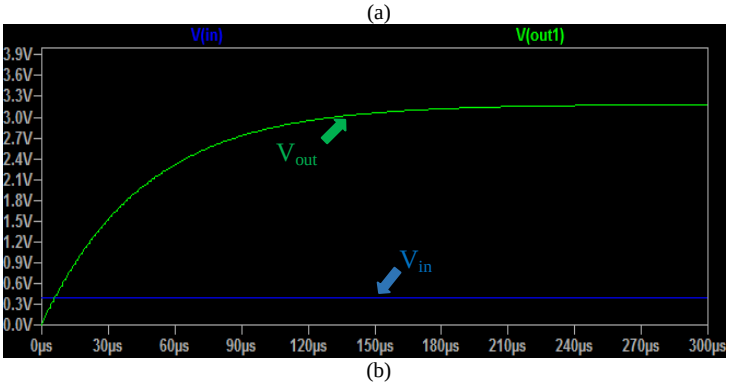


Fig. 7. Simulated ripple voltage as a function of the output power.



(a)



(b)

Fig. 8. Simulated output voltage as a function of time: (a) proposed converter and (b) Fibonacci converter.

6. Conclusion

To prevent problems with energy shortages by utilizing energy harvesting systems, a three parallel-connected Fibonacci SC dc-dc converter has been proposed in this paper. The result of theoretical and simulation substantiated the following results: First, by using a three parallel-connected structure based on the Fibonacci-type converter, the proposed converter can achieve higher voltage gains and higher power efficiency. Secondly, the stepped-up electric charge of the output capacitor of the proposed converter was evoked in every clock cycle. Thus, the proposed converter can minimize its size, because it can connect with a small output capacitor untroubled from ripple noise. For this reason, the size of the proposed converter will become smaller than that of the traditional Fibonacci converter. Lastly, the response speed of the proposed converter was faster than the traditional Fibonacci converter. In future studies, further experiments will be conducted to confirm the simulated results with the aim of improving the proposed converter circuit to become a chip.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Ratanaubol Rubpongse wrote the paper and simulated data; Takaaki Ishibashi co-wrote and revised the paper; Wanglok Do carried out experiments; Farzin Asadi supervised technical aspects; Kei Eguchi developed the concept; All authors had approved the final version.

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