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Implementation of improved positive and negative sequences separation phase-locked loop under grid voltage sags

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Abstract

Detecting and locking the phase and frequency information of the voltage at point of common coupling (PCC) quickly and accurately under grid voltage sags is the premise of grid connected inverter which can ride through the fault successfully. In order to achieve grid voltage synchronize with phase and frequency information quickly under voltage sags, this paper proposed an improved Phase-Locked Loop (PLL), which is referred to as DSCαβ-PLL, based on the stationary references frame PLL. The DSCαβ-PLL can separate and track the positive-sequence voltage component of PCC in the stationary references frame. Then the proposed method is deduced in detail, and math expressions are presented next. According to above improvements, the relevant PLL simulation model is built in MATLAB/Simulink. The results show that the DSCαβ-PLL can not only be stable in different types of voltage sags, but also can track and lock the phase and frequency information of the voltage at PCC fast.

Keywords: Voltage sag; phase-locked loop; positive sequence separation; symmetrical components method

1. Introduction

Renewable Energy Systems (REGs), such as solar energy systems, wind energy systems and geothermal energy systems have been attracting more and more attention in recent years due to the increasing depletion of fossil fuels. The grid-connected inverter is an important interface module which can connect the renewable generation unit to the power grid in REGs. However, the high permeability of REG makes the structure of the power system network more complicated. Faced with the most common faults in power system--voltage sags, the REG should have Low Voltage Ride Through (LVRT) capability in order to run continuously when faults and disturbances occur [1]-[3].

Since the LVRT control strategy of grid-connected inverter is usually implemented in Synchronous Reference Frame (SRF), it is become more and more important that the inverter can obtain the phase and frequency information of the fundamental positive sequence voltage of the grid quickly and accurately under voltage sags.

Phase-Locked Loop (PLL) is recommended to be applied in order to realize synchronization and the appropriate operation from grid-connected inverter. The existing PLL algorithms generally divided into hardware PLL and software PLL. The realization of hardware PLL is to obtain phase and frequency information by the zero voltage crossing point detection of grid voltage in hardware circuits. However, in practice, due to a limited number of zero-crossing points and the noise caused by the non-ideal experimental conditions, there is a large error between the detected phase information of hardware PLL and the actual phase of fundamental positive-sequence voltage of the grid. For this case, it is difficult to lock phase of power grid.

The software PLL mainly includes SRF PLL (dq-PLL) [4], the decoupled double SRF PLL (ddq-PLL) [5], and the stationary reference frame PLL (αβ-PLL) [6]. The PLL method based on general delayed

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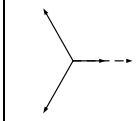
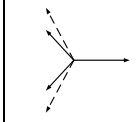
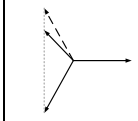
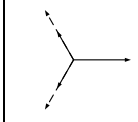
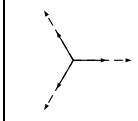
signal cancelation (GDSC-PLL) [7], [8]can detect and eliminate the specified harmonic components, but the main feedback loop of this scheme has serious nonlinearity, which makes it difficult to guarantee the stability of the system. In order to solve this problem, an enhanced general delayed signal cancellation PLL (EGDSC-PLL) [9] was proposed, although this method avoids the effect of nonlinearity on the stability of the system, it used the integral of power frequency to be the reference of park transformation, which will make system unable to lock phase of fundamental positive-sequence voltage accurately under voltage phase jump.

To ensure that the REG can acquire and lock the phase and frequency information of grid voltage under different types of voltage sags accurately and quickly, an improved PLL technique was proposed in this paper. Firstly, this paper analyzes the fault types of voltage sags, and the influence of each sequence component in the stationary reference frame is derived by theoretical deduction. Then the fundamental positive-sequence voltage is obtained, combining with αβ-PLL, frequency and phase information of power grid is locked. According to above improvements, the relevant PLL model is built in MATLAB/Simulink. The results show that the proposed PLL algorithm can not only be stable in different types of voltage sag, but also fast track and lock the phase and frequency information of the PCC voltage fast.

Table 1. Classification of each type of voltage sag

Type	Voltage Shape	Fault Description	Vector Description	Zero Sequence Voltage
a		Single-phase fault	$v_a = X$ $v_b = -\frac{1}{2}E - j\frac{\sqrt{3}}{2}E$ $v_b = -\frac{1}{2}E + j\frac{\sqrt{3}}{2}E$	$0.333(X-E)$
b		Two-phase fault (without phase jump)	$v_a = E$ $v_b = -\frac{1}{2}E - j\frac{\sqrt{3}}{2}V$ $v_b = -\frac{1}{2}E + j\frac{\sqrt{3}}{2}V$	0
c		Two-phase fault (with phase jump)	$v_a = E$ $v_b = -\frac{1}{2}E - j\frac{\sqrt{3}}{2}E$ $v_b = -\frac{1}{2}E + j\frac{\sqrt{3}}{2}V$	$0.289(V-E)$
d		Two-phase grounded fault	$v_a = E$ $v_b = -\frac{1}{2}X - j\frac{\sqrt{3}}{2}X$ $v_b = -\frac{1}{2}X + j\frac{\sqrt{3}}{2}X$	$0.333(E-X)$
e		Three-phase fault	$v_a = V$ $v_b = -\frac{1}{2}V - j\frac{\sqrt{3}}{2}V$ $v_b = -\frac{1}{2}V + j\frac{\sqrt{3}}{2}V$	0

2. Voltage Sag Classification Algorithm

The proposed voltage sag classification algorithm uses voltage vector analysis of positive and negative sequences of PCC voltage, due to the different types of voltage sags and their characteristics. The classification algorithm manages to classify the voltage sags into five different types (type a-e), according to [10]. The single-phase voltage sag is described as type a, two-phase voltage sags is represented as type b-d (including different phase jumps of voltage) and three-phase voltage sag is described as type e. The

proposed classification of each type of voltage sag is shown in Table 1, where E means nominal voltage of PCC, and V means residual voltage of PCC.

According to the symmetrical components method, the phase voltage of grid under voltage sag can be described as follows:

$$\begin{aligned} u_{si} &= u_{si}^{+} + u_{si}^{-} + u_{si}^{0} \\ &= U_s^{+}\cos(\omega t - k\frac{2\pi}{3}) + U_s^{-}\cos(-\omega t - k\frac{2\pi}{3} + \varphi^{-1}) \\ &+ U_s^{0}\cos(\omega t + \varphi^{0}) \end{aligned} \tag{1}$$

where k=0,1,2 when i=a, b, c, U_s^{+}, U_s^{-} and U_s^{0} are the amplitude of positive-, negative- and zero-sequence voltage.

The three phase voltage use the equations of the Clarke transformation, as shown in the following, to translate the *abc* natural rotating reference frame into the $\alpha\beta\gamma$ stationary reference frame:

$$u_{s\atop(\alpha\beta\gamma)} = \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \\ u_{s\gamma} \end{bmatrix} = T_{\alpha\beta\gamma}\begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix} \tag{2}$$

$$u_{s\atop(\alpha\beta\gamma)} = \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \\ u_{s\gamma} \end{bmatrix} = T_{\alpha\beta\gamma}\begin{bmatrix} u_{sa}^{+} + u_{sa}^{-} + u_{sa}^{0} \\ u_{sb}^{+} + u_{sb}^{-} + u_{sb}^{0} \\ u_{sc}^{+} + u_{sc}^{-} + u_{sc}^{0} \end{bmatrix} \tag{3}$$

where

$$T_{\alpha\beta\gamma} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4}$$

The sequence components in $\alpha\beta\gamma$ stationary reference frame are derived by substituting (1) into (3):

$$\begin{cases} u_{s\alpha}^{+} = \frac{2}{3}U_s^{+}\cos(\omega t) - \frac{1}{3}U_s^{+}\cos(\omega t - \frac{2\pi}{3}) - \frac{1}{3}U_s^{+}\cos(\omega t - \frac{4\pi}{3}) \\ u_{s\beta}^{+} = \frac{\sqrt{3}}{3}U_s^{+}\cos(\omega t - \frac{2\pi}{3}) - \frac{\sqrt{3}}{3}U_s^{+}\cos(\omega t - \frac{4\pi}{3}) \\ u_{s\gamma}^{+} = 0 \end{cases} \tag{5a}$$

$$\begin{cases} u_{s\alpha}^{-} = \frac{2}{3}U_s^{-}\cos(-\omega t + \varphi^{-1}) - \frac{1}{3}U_s^{-}\cos(-\omega t - \frac{2\pi}{3} + \varphi^{-1}) - \frac{1}{3}U_s^{-}\cos(-\omega t - \frac{4\pi}{3} + \varphi^{-1}) \\ u_{s\beta}^{-} = \frac{\sqrt{3}}{3}U_s^{-}\cos(-\omega t - \frac{2\pi}{3} + \varphi^{-1}) - \frac{\sqrt{3}}{3}U_s^{-}\cos(-\omega t - \frac{4\pi}{3} + \varphi^{-1}) \\ u_{s\gamma}^{-} = 0 \end{cases} \tag{5b}$$

$$\begin{cases} u_{s\alpha}^{0} = 0 \\ u_{s\beta}^{0} = 0 \\ u_{s\gamma}^{0} = U_{s}^{0}\cos(\omega t + \varphi^{0}) \end{cases} \tag{5c}$$

where the positive-sequence components $u_{s\alpha}^{+}$, $u_{s\beta}^{+}$ are rotated at a positive angular velocity ω, and the negative-sequence components $u_{s\alpha}^{-}$, $u_{s\beta}^{-}$ are rotated at a positive angular velocity $-\omega$.

According to (6a) and (6b), the γ–sequence components $u_{s\gamma}^{+}$ and $u_{s\gamma}^{-}$ are equal to zero, that is to illustrate that, when the grid occurs voltage sags, the zero-sequence voltage has no influence on positive- and negative-sequence separation in the $\alpha\beta\gamma$ stationary reference frame, no matter whether there are zero-sequence components in the *abc* natural rotating reference frame. Therefore, γ–sequence components $u_{s\gamma}^{+}$ and $u_{s\gamma}^{-}$ can be avoided either.

3. Proposed PLL System

The proposed system is shown in Fig. 2. The idea is to use an open-loop positive and negative sequences separation method as the input of a closed-loop PLL algorithm to build a new combined PLL system which is referred to as DSCαβ-PLL. This new combined PLL system point at operating accurately and quickly under balanced and unbalanced voltage sags and also at obtaining a lower frequency and phase overshoot than conventional PLL.

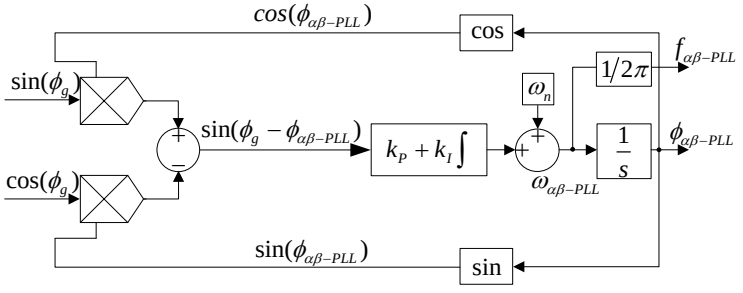


Fig. 1. Closed-loop diagram of the αβ-PLL.

3.1. PLL based on αβ stationary reference frame(αβ-PLL)

The closed-loop diagram of αβ−PLL is shown in Fig. 1. The input of αβ−PLL is shown as follows:

$$\begin{aligned} \sin(\phi_g) &= \frac{u_\beta}{\sqrt{u_\alpha^2 + u_\beta^2}} \\ \cos(\phi_g) &= \frac{u_\alpha}{\sqrt{u_\alpha^2 + u_\beta^2}} \end{aligned} \tag{6}$$

where ϕ_g is the phase angle of actual power grid, u_α and u_β are the grid voltage components in stationary αβ reference frame.

Trigonometric equations are applied in order to obtain the output phase angle $\phi_{\alpha\beta-PLL}$ and the output frequency $f_{\alpha\beta-PLL}$ which is shown in (7). It should be noted that (7) is established if $\Delta\phi$ is small

$$\begin{aligned}&\Delta\phi=\phi_g-\phi_{\alpha\beta-PLL}\cong\sin(\phi_g-\phi_{\alpha\beta-PLL})\\&\Leftrightarrow\Delta\phi\cong\sin(\phi_g)\cos(\phi_{\alpha\beta-PLL})-\sin(\phi_{\alpha\beta-PLL})\cos(\phi_g)\end{aligned}\tag{7}$$

The principle of the αβ−PLL is to reduce the sinus of the difference $\Delta\phi$, which is between grid phase angle ϕ_g and the output phase angle of αβ−PLL $\phi_{\alpha\beta-PLL}$, to zero by using a PI-controller, and thus locking the phase to the power grid. The output frequency $f_{\alpha\beta-PLL}$ can be obtained by performing a complementation calculation on the output angular frequency of PLL $\omega_{\alpha\beta-PLL}$ for 2π.

When balanced voltage sag occurs, at the same setting time, the overshoot of αβ−PLL on frequency estimation is always lower than those other two PLLs (dq-PLL and ddq-PLL) [11].

However, when unbalanced voltage sags appear, because the unbalanced voltage vector consists of negative sequence component, the PLL bandwidth can be reduced to reach a negligible effect. Therefore, in this situation, the conventional αβ−PLL technique is not the most appropriate solution for the control of tracking phase angle and frequency of the fundamental positive-sequence voltage of the grid.

3.2. Positive and negative sequences separation based on delayed signal cancellation(DSC) technique

According to Table I, when the voltage sags occur, there are non-positive sequence components in the system (negative- and zero-sequence). In order to ensure that the PLL enable accurately and quickly obtain the phase and frequency of the fundamental positive sequence voltage of the grid, even under unbalanced voltage sags, negative- and zero-sequence component should be ignored in the control strategy.

For the purpose of solving the transient instability problem of conventional αβ−PLL, the positive negative sequences separation based on delayed signal cancellation (DSC) technique is introduced [12].

According to (5), the zero-sequence voltage has no influence on positive and negative sequences separation in the $\alpha\beta\gamma$ stationary reference frame, furthermore, the expression of voltage vector can be obtained in $\alpha\beta$ stationary reference frame by (5):

$$\begin{aligned}u_{s\atop(\alpha\beta)}&=\begin{bmatrix}u_{s\alpha}\\u_{s\beta}\end{bmatrix}=u_{s\atop(\alpha\beta)}^{+}+u_{s\atop(\alpha\beta)}^{-}+u_{s\atop(\alpha\beta)}^{0}\\&=U_s^{+}\begin{bmatrix}\cos(\omega t)\\\sin(\omega t)\end{bmatrix}+U_s^{-}\begin{bmatrix}\cos(-\omega t+\varphi^{-1})\\\sin(-\omega t+\varphi^{-1})\end{bmatrix}\end{aligned}\tag{8}$$

After 1/4 fundamental cycle delay in (8):

$$\begin{cases}u_{s\alpha}(t-T/4)=\;\;U_s^{+}\sin(\omega t)-U_s^{-}\sin(-\omega t+\varphi^{-1})\\u_{s\beta}(t-T/4)=-U_s^{+}\cos(\omega t)+U_s^{-}\cos(-\omega t+\varphi^{-1})\end{cases}\tag{9}$$

The positive- and negative-sequence components voltage of grid can be achieved in $\alpha\beta$ stationary reference frame with addition and subtraction equations:

$$\begin{cases}u_{s\alpha}^{+}=1/2[u_{s\alpha}(t)-u_{s\beta}(t-T/4)]\\u_{s\alpha}^{-}=1/2[u_{s\beta}(t)+u_{s\alpha}(t-T/4)]\\u_{s\beta}^{+}=1/2[u_{s\alpha}(t)+u_{s\beta}(t-T/4)]\\u_{s\beta}^{-}=1/2[u_{s\beta}(t)-u_{s\alpha}(t-T/4)]\end{cases}\tag{10}$$

3.3. Proposed new combined PLL

It can be seen from the preceding paragraph, because of the negative existed in the unbalanced voltage vector, the conventional αβ−PLL technique has the fatal weakness under unbalanced voltage sags. At the same time, DSC technique can accurately separate positive- and negative-sequence voltage of the grid.

The proposed new combined PLL DSCαβ-PLL is the composite of the decoupling separation unit is used in DSC to separate positive- and negative-sequence voltage of the grid and the αβ-PLL algorithm (Fig. 1) to track and lock the phase angle as well as frequency of the grid voltage. The new PLL method offers lower phase angle and frequency overshoot than the conventional PLL method. The structure of proposed new combined PLL is shown in Fig. 2.

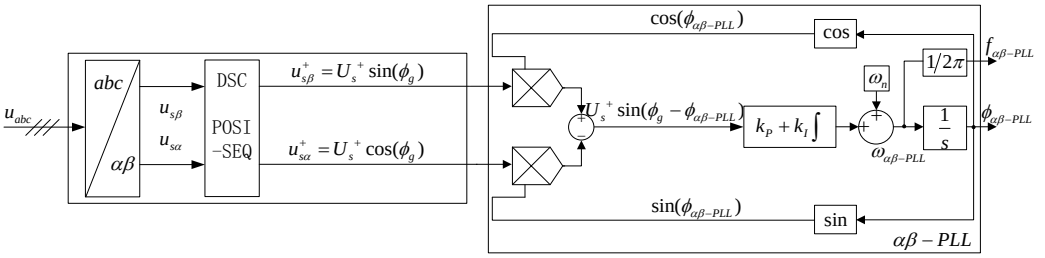


Fig. 2. Structure of new combined PLL DSCαβ-PLL.

The small-signal model of the proposed DSCαβ-PLL, conventional αβ-PLL and DSCdq-PLL were established, and then frequency domain analysis was performed under the same parameters to obtain the magnitude-frequency response of the three types of PLL algorithm, the result is shown in Fig. 3.

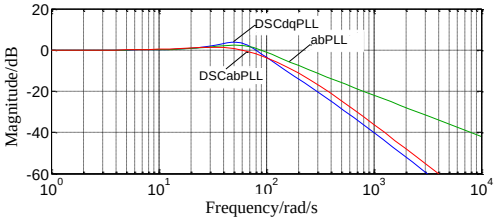


Fig. 3. Magnitude-frequency response of the three types of PLL algorithm.

According to Fig. 3, the proposed DSCαβ-PLL achieve a resonance peak of 1.37dB at the frequency of 31.6Hz, the conventional αβ-PLL achieve a resonance peak of 2.44dB at the frequency of 51Hz and the conventional DSCdq-PLL achieve a resonance peak of 3.82dB at the frequency of 52.2Hz.

As a result of the resonance peak is positively correlated with overshoot, it can be seen from the magnitude-frequency response that the proposed DSCαβ-PLL has a lower overshoot instead of the conventional PLL αβ-PLL and DSCdq-PLL.

4. Simulation Results

In this section, a comparison of the new proposed DSCαβ-PLL to the other PLLs is shown in order to validate its advantages. The simulation focus on DSCαβ-PLL, αβ-PLL and DSCdq-PLL, which are operate in the balanced and unbalanced voltage sags. These numerical simulations were obtained from MATLAB/Simulink models.

4.1. Performance of three PLLs under single-phase voltage sag and phase jump

The simulation conditions of each waveform in Fig. 4 are as follows: an unbalanced fault with 66.7% voltage sag and a 30 degree phase lead on phase a occurs at 1s.

Fig. 4 (a) shows the simulation waveform of the grid voltage under single-phase voltage sag and phase changed;

Fig. 4 (b) shows the output frequency simulation waveform comparison of new proposed DSCαβ-PLL to the other two PLLs. It can be seen from the waveform that DSCdq-PLL locks the grid frequency need more than 1.6% overshoot compared with the proposed PLL under single-phase voltage sag with phase jump in the grid. And because of negative-sequence in the voltage, αβ-PLL cannot lock the phase angle and frequency accurately.

Fig. 4 (c) shows the comparison waveform of the fundamental positive-sequence voltage of the phase a and output phase angle of the proposed PLL. As can be obtained from the figure, when the single-phase voltage sag with phase jump occurs, the proposed DSCαβ-PLL can lock the phase angle of the grid in a very short period of time.

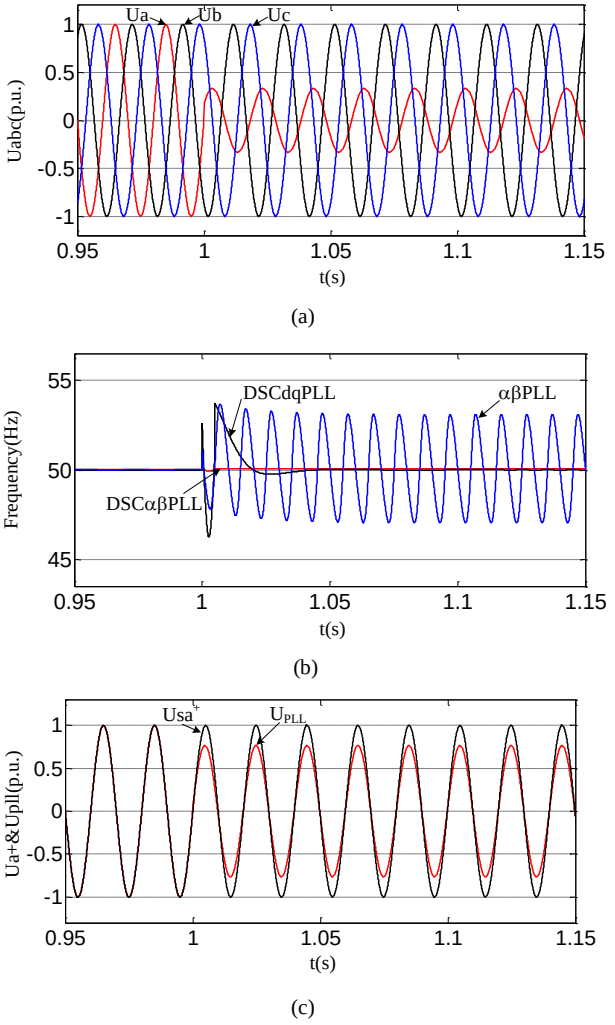


Fig. 4. Simulation waveform under sigle-phase voltage sag with phase jump:(a) grid voltage, (b) the comprision of output frequency, (c) the comprision of output phase angle.

4.2. Performance of three PLLs under two-phase voltage sag and phase jump

The simulation conditions of each waveform in Fig. 5 are as follows: an unbalanced fault with 43.3% voltage sag and 18 degree phase lead on phase b, and an unbalanced fault with 55.5% voltage sag and 29 degree phase lag on phase c occurs at 1s.

Fig. 5 (a) shows the simulation waveform of the grid voltage under two-phase voltage sag and phase changed;

Fig. 5 (b) shows the output frequency simulation waveform comparison of new proposed DSCαβ-PLL to the other PLLs. It can be seen from the waveform that DSCdq-PLL locks the grid frequency need more than 1.93% overshoot and 0.5 cycle time compared with the proposed PLL under two-phase voltage sag with phase jump in the grid. And because of negative-sequence in the voltage, αβ-PLL cannot lock the phase angle and frequency accurately.

Fig. 5 (c) shows the comparison waveform of the fundamental positive-sequence voltage of the phase a and output phase angle of the proposed PLL. As can be obtained from the figure, when the two-phase voltage sag with phase jump occurs, the proposed DSCαβ-PLL can lock the phase angle of the grid in a very short period of time.

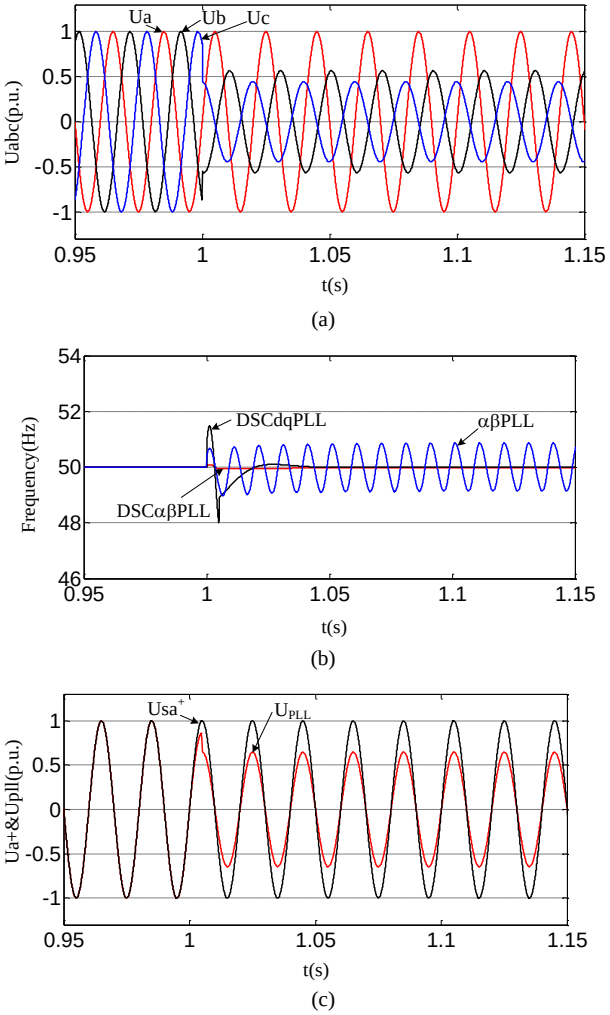


Fig. 5. Simulation waveform under two-phase voltage sag with phase jump:(a) grid voltage, (b) the comprision of output frequency, (c) the comprision of output phase angle.

4.3. Performance of three PLLs under three-phase voltage sag and frequency jump

The simulation conditions of each waveform in Fig. 6 are as follows: a balanced fault with 66.7% voltage sag and frequency jump on each phase occurs at 1s.

Fig. 6 (a) shows the simulation waveform of the grid voltage under three-phase voltage sag and frequency changed;

Fig. 6 (b) shows the output frequency simulation waveform comparison of new proposed DSCαβ-PLL

to the other PLLs. It can be seen from the waveform that DSCdq-PLL locks the grid frequency need more than 0.5% overshoot and 1 cycle time compared with the proposed PLL under three-phase voltage sag with frequency jump in the grid. And because there is no negative-sequence in the voltage, αβ-PLL can remain its advantages.

Fig. 6 (c) shows the comparison waveform of the fundamental positive-sequence voltage of the phase a and output frequency of the proposed PLL. As can be obtained from the figure, when the three-phase voltage sag with frequency jump occurs, the proposed DSCαβ-PLL can lock the phase angle of the grid in a very short period of time.

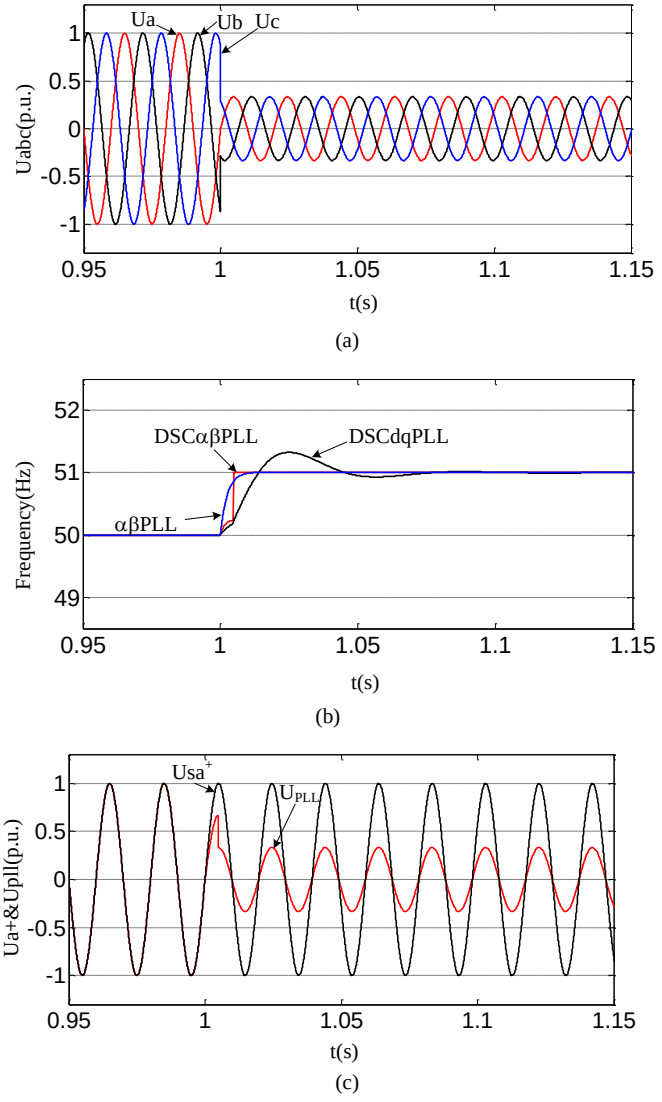


Fig. 6. Simulation waveform under three-phase voltage sag with frequency jump:(a) grid voltage, (b) the comprision of output frequency, (c) the comprision of output phase angle.

5. Conclusion

In this paper, the classification of different types of voltage sags is proposed, and the paper illustrates that when the grid occurs voltage sags, the zero-sequence voltage has no influence on positive and negative sequences separation in the $\alpha\beta\gamma$ stationary reference frame, no matter whether there are zero-

sequence components in the *abc* natural rotating reference frame. Therefore, γ–sequence components $u_{s\gamma}^{+}$ and $u_{s\gamma}^{-}$ can be avoided to simplify the calculation.

Combining with the DSC positive and negative sequences separation technique and conventional αβ-PLL algorithm, an improved new PLL DSCαβ-PLL was proposed in this paper. The proposed new combined PLL can separate and track the positive-sequence voltage component of grid in the stationary references frame and have lower overshoot and response time than the conventional PLLs.

Based on the above conclusion, the improved new PLL DSCαβ-PLL proposed in the paper shows the capability to track and lock the phase of the grid steadily, accurately and rapidly in the transient process of different kinds of voltage sags. The simulation results also verify the feasibility and correctness of the proposed scheme.

Acknowledgement

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